Electrical Engineering - Optional For IAS (UPSC)

Digital Electronics - 2015-2021

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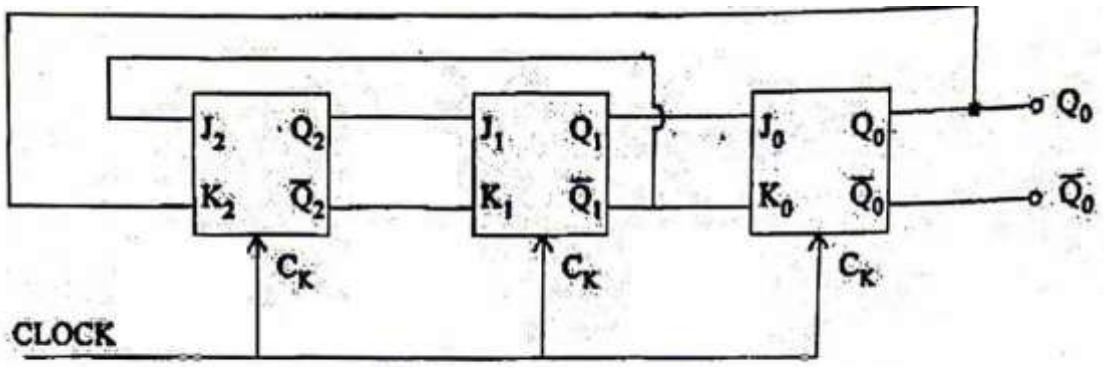
UPSC – ELECTRICAL Engineering optional – 2015 Questions

1. Obtain all the possible minimal functions for: $F = \sum(0, 2, 3, 4, 5, 7)$. **[10M]**

2. Divide by N counter is shown in the figure below. If Initially $Q_0 = 0, Q_1 = 1, Q_2 = 0$, what is the value of N? **[20M]**



Figure

UPSC – ELECTRICAL Engineering optional – 2016 Questions

1. Minimize the SOP terms given for a Boolean function $f(A, B, C, D) = \sum m(2, 3, 8, 10, 11, 12, 14, 15)$

Implement the minimized function using NAND gates alone. **[10M]**

2. What is a PLA? Realize the following functions using an appropriate PLA: [**10M]**

$$f_1 = AB + CD$$
$$f_2 = \bar{A}B + A\bar{B}$$
$$f_3 = AD + BC + \bar{B}D$$

UPSC – ELECTRICAL Engineering optional – 2017 Questions

1. For the Boolean function $F(W, X, Y, Z) = \sum(0, 2, 5, 6, 7, 8, 10, 13)$ **[20M]**

(i) find all the prime implicants;

(ii) give minimal representation;

(iii) find minimal two-level realization using NAND gates only.

2. Prove that $\bar{A}B + \bar{B}C + \bar{A}C = \bar{A}B + \bar{B}C$. **[10M]**

3. Find the state transition diagram and realization using J-K flip-flops to count Mod 7 in the following sequence: $000, 001, 011, 100, 101, 111$ **[20M]**

UPSC – ELECTRICAL Engineering optional – 2018 Questions

1. Convert the following logic equation to NAND logic and draw the circuit using NAND gates:$Z = (\overline{A + B}) + C + A(\overline{B + C})$ **[20M]**

2. Convert a D flip flop to function as an S-R flip flop .Draw the circuit. **[10M]**

3. Design a synchronous counter using D flip flop that counts in the following sequence:

$$6, 3, 5, 0, 2, 6, 3, 5, 0, 2, 6, \ldots$$

Draw the circuit. **[20M]**

UPSC – ELECTRICAL Engineering optional – 2019 Questions

1. Simplify the following expression using Boolean algebra: **[10M]**

$$\mathrm{Y = AC + A(B + C) + C(B + C)}$$

and draw the logic diagram for reduced expression.

2. Implement Astable Multi vibrator using NAND gates and explain its operation. **[10M]**

3. Reduce the combinational logic circuit shown in Figure 7(d) to a minimum form. **[10M]**

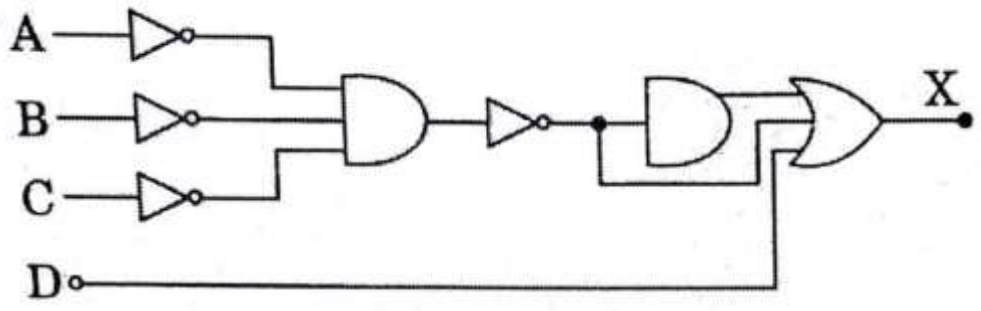


Figure 3.

4. Draw the block diagram of a single slope type A/D converter and explain its principle of operation. **[20M]**

UPSC – ELECTRICAL Engineering optional – 2020 Questions

1. Implement the following Boolean functions with a 4 × 3 Programmable Logic Array (PLA): **[10M]**

$F_1 = \bar{B}\bar{C} + A\bar{B}$

$F_2 = AB\bar{C} + A\bar{B}C\bar{D}$

$F_3 = \bar{A}\bar{B}\bar{C}D + A\bar{B}CD$

2. Design a combinational circuit to implement the minimal sum-of-products of the logic function $F = \sum_{WXYZ}(1,\ 2,\ 3,\ 4,\ 5,\ 7,\ 11,\ 13)$. **[10M]**

3. Design a synchronous sequential circuit with D-flip-flops for a state diagram shown in Figure 4(b). **[20M]**

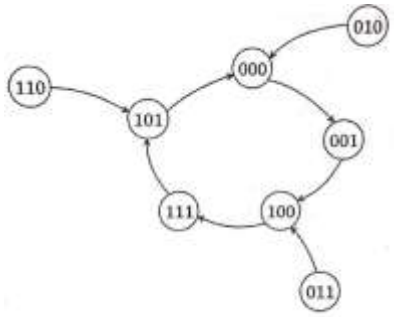


Figure 4(b)

UPSC – ELECTRICAL Engineering optional – 2021 Questions

1. Consider the four variables logic function defined as follows:

$F(A, B, C, D) = \overline{A}C + \overline{A}D + \overline{B}C + \overline{B}D + AB\overline{C}\overline{D}$

Assuming input variables as A, B, C and D, propose a logic circuit using only three logic gates to implement the function. **[10M]**

2. Consider the circuit shown in Figure 2(c) below. Let inputs A, B and C be all initially LOW. Output Y is supposed to go HIGH only when A, B and C go HIGH in a certain sequence. Determine the sequence that will make Y go HIGH. Modify this circuit to use D-Flip-flops. **[10M]**

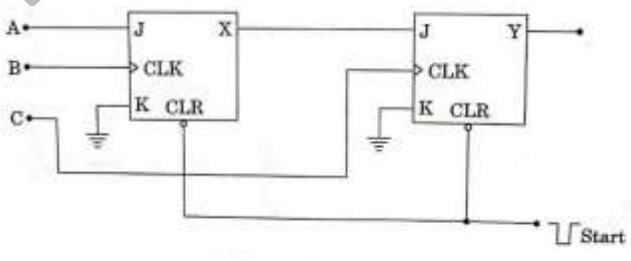


Figure 2(c)

3. **(i)** Verify by determining the logic equation for the output and by constructing the truth table for the logic circuit shown in Figure 4(b).

(ii) Use an 8 to 1 multiplexer and logic gates to implement the following function: **[20M]**

$$F(A, B, C, D, E) = \sum m(0, 1, 2, 4, 5, 6, 7, 13, 14, 20, 21, .., 28, 29, 30, 31)$$

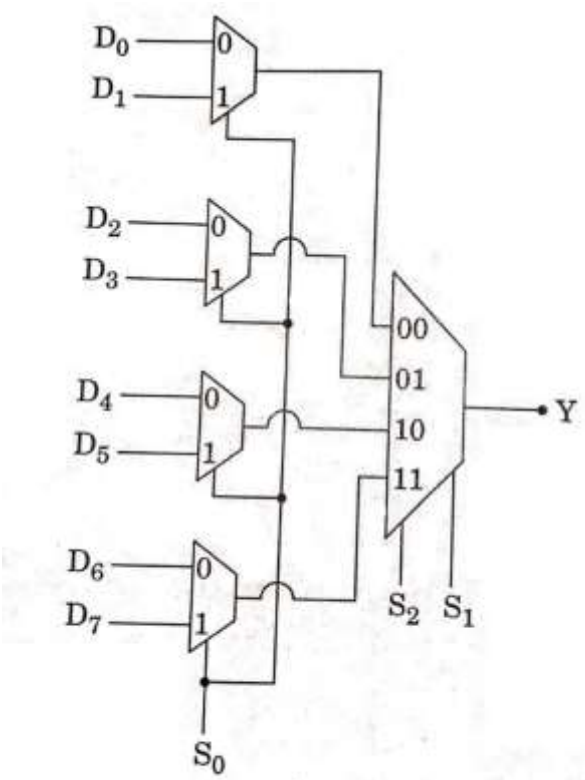


Figure 4(b)