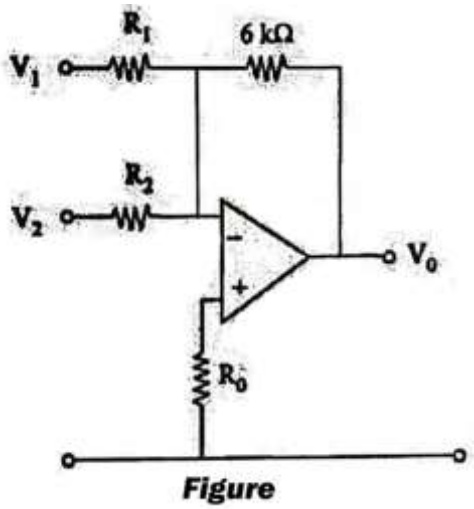
Electrical Engineering - Optional For IAS (UPSC)

Analog Electronics - 2015-2021

INDIANCIVILS.COM - 90000 18804

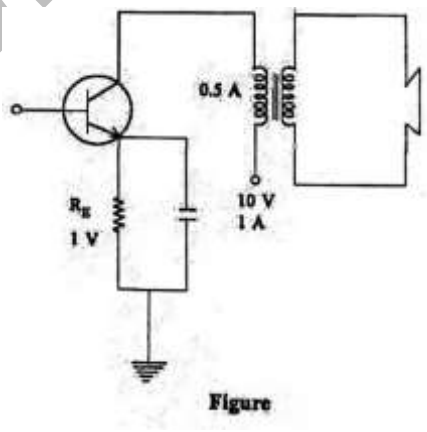
UPSC – ELECTRICAL Engineering optional – 2015 Questions

1. In the Figure shown what is the function of R_0 and determine its value when $V_0 = -3V_1 - 2V_2$. **[10M]**



Figure

2. Find the efficiency of a class A amplifier shown in Figure. Given that the voltage drop across R_E is 1 V, the signal current swings from -0.5 A to $+0.5$ A and the DC current is 1 A. **[10M]**



Figure

3. Explain the speed enhancement gained in MOS device by using silicon-on-sapphire or spinel (SOS). What are the other good features of the process? Mention the drawbacks. **[20M]**

UPSC – ELECTRICAL Engineering optional – 2016 Questions

1. Two ideal and identical junction diodes are connected as shown in Fig. 1(d). If the current through the reverse-biased diode is I_0 and is constant, explain the circuit operation when both the diodes are connected in forward-biased condition. Assume $V_T = 25\text{mV}$, $V_\gamma = 0.7\ V\ and\ \eta = 1$ for the diodes. **[10M]**

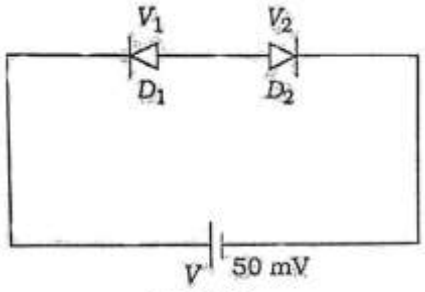


Fig. 1(d)

2. For the circuit shown in Fig. 2(c), calculate the resistance R_0 as seen by the output terminals. Ignore the effect of $R_1$and R_2. Assume $\beta = 99\ and\ h_{ie} = 1\ \text{k}\Omega$. Comment on the value of R_0 of the circuit: **[10M]**

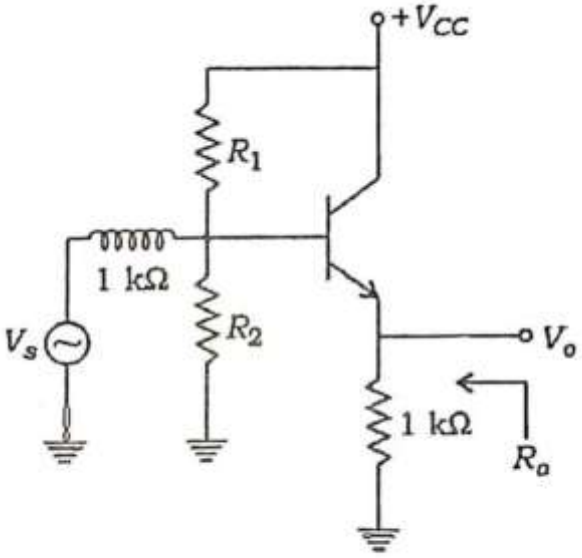


Fig. 2(c)

3.For the circuit shown in Fig. 3(c), get the expression for V_0. Also sketch the output waveform. Assume that the op-amp is ideal. $R = \sqrt{\frac{L}{C}}, \omega = \frac{1}{\sqrt{LC}}$ and $V_i = 10 \sin \omega t$: **[10M]**

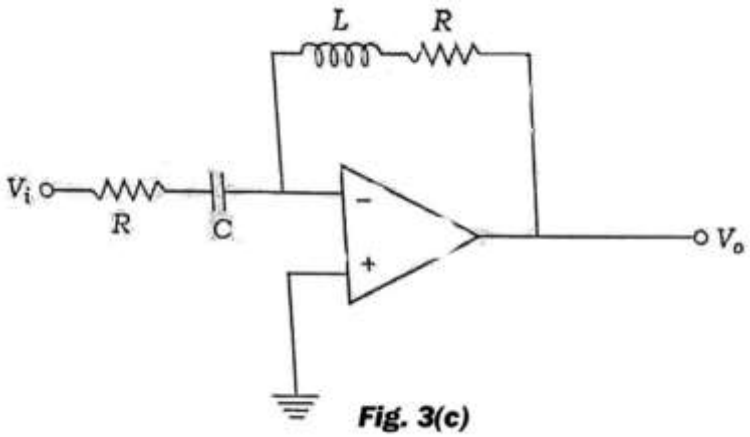


Fig. 3(c)

4. For the op-amp circuit shown in Fig. 4(c), deduce the output voltage expression. Calculate V_0, when $R_1 = 1\ k\Omega = R_2$, $R_3 = 1$ K and $R_4 = 2$ K and $V_{in} = 1$ V **[10M]**

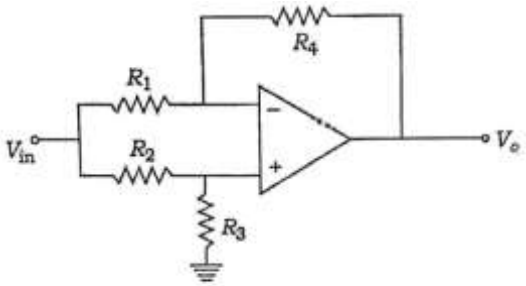


Fig. 4(c)

5. Identify the circuit shown in Fig. 6(a). Briefly explain the same. Calculate the current i and V_o, if $V_R = 5$ V and $R = 5\ k\Omega = R_F$: **[20M]**

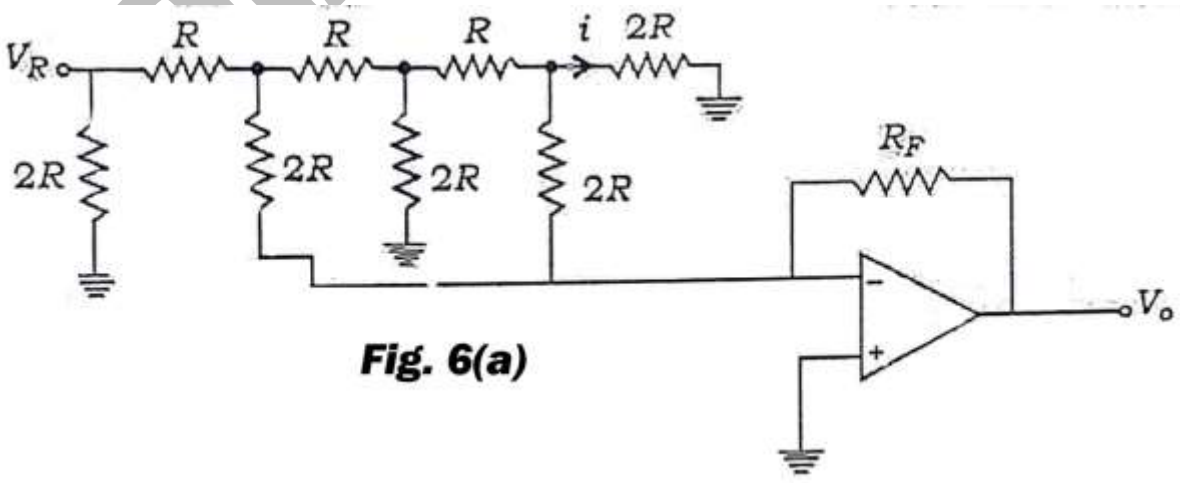


Fig. 6(a)

UPSC – ELECTRICAL Engineering optional – 2017 Questions

1. For the circuit given in Fig. 1(d)–

(i) draw the input and output waveforms;

(ii) find the average value of the output voltage waveform.

Assume that the diode in the circuit is ideal. **[10M]**

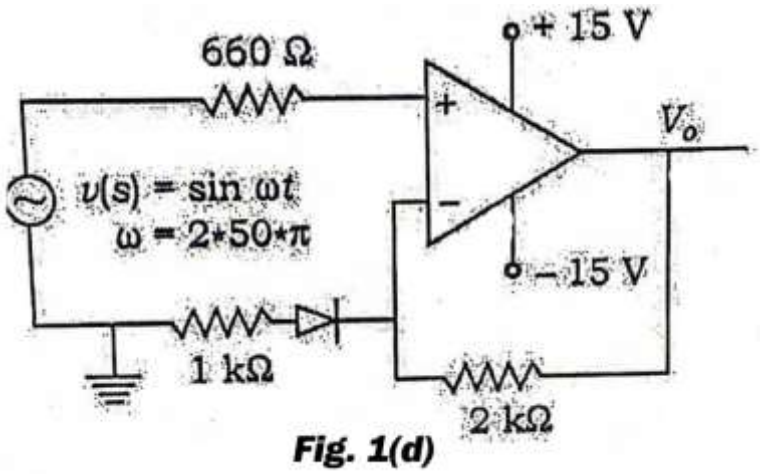


Fig. 1(d)

2. Find the average voltage at the point V_0 in the circuit given in Fig. 4(c): **[10M]**

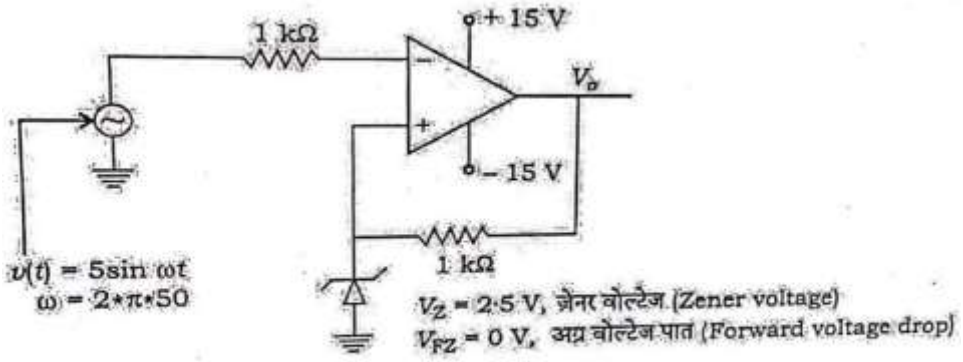


Fig. 4(c)

3. (i) Draw the circuit diagram of Wien bridge oscillator using OP-AMP.

(ii) Find the value of R to get a sustained oscillation of 1115 Hz. Assume that the value of the capacitor is 0.1μF. **[10M]**

4. (i) Draw the circuit diagram of a bandpass filter using OP-AMP. Its parameters are $f_L = 300\ Hz,\ f_H = 2\ kHz$ and passband gain is 4.

(ii) Calculate the value of Q. Assume that the capacitor value is 0.01μF. **[20M]**

UPSC – ELECTRICAL Engineering optional – 2018 Questions

1. For the op-amp circuit shown in Figure 1(d), determine the gain $A_v = \frac{V_0}{V_i}$. Assume that all resistors are equal. **[10M]**

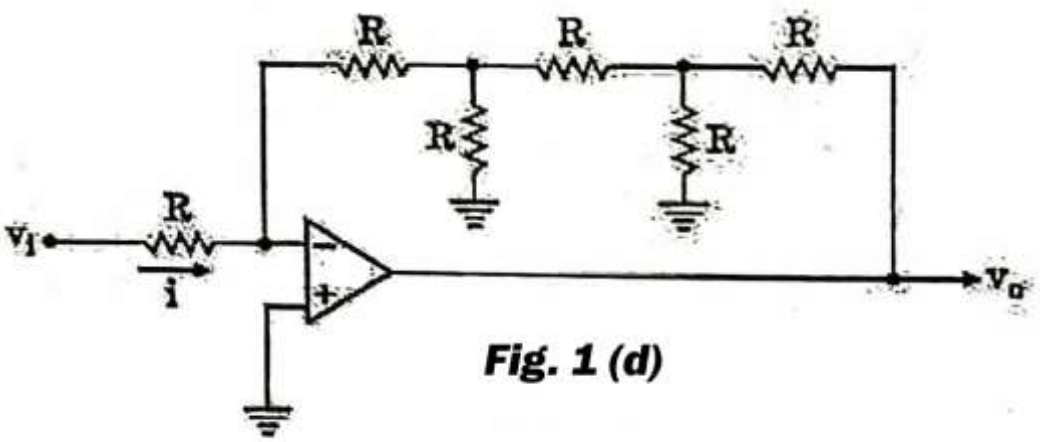


Fig. 1 (d)

2. Determine the feedback fraction and the operating frequency for the oscillator circuit shown in Figure 6(c) **[10M]**

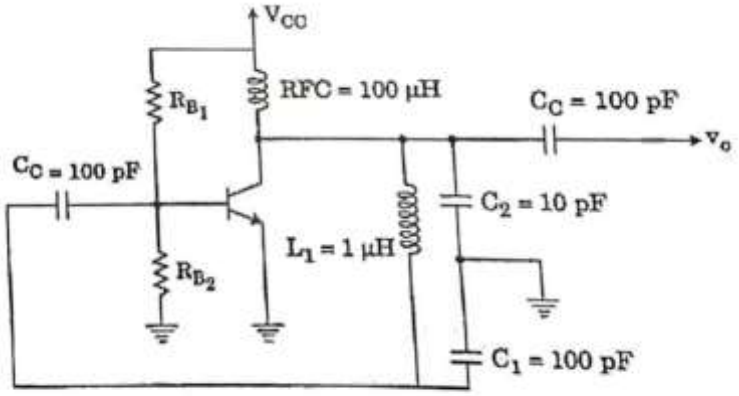


Figure 6(c)

3. The integrator circuit shown in Figure 4(c) is to be used to generate a triangular waveform from a 500 Hz square wave connected to its input. Suppose that the square wave alternates between ± 12 V.

(i) Find the minimum slew rate required for the amplifier.

(ii) Find the maximum output voltage the amplifier can generate. **[10M]**

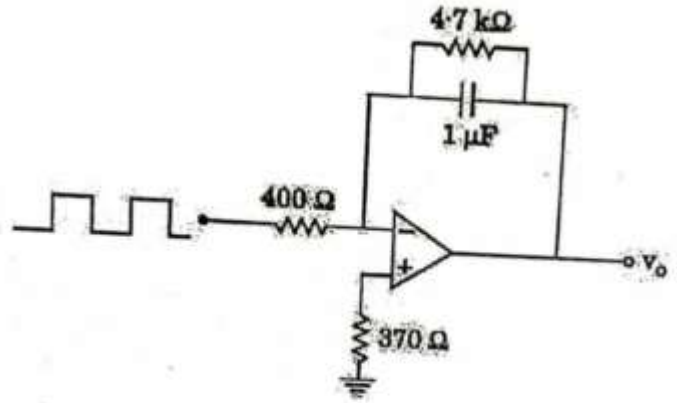


Fig. 4(c)

4. Calculate the output voltage V_0 in terms of the input voltagesv_{i1}, v_{i2}, v_{i3} and v_{i4} for the circuit shown in Figure 8(b). **[20M]**

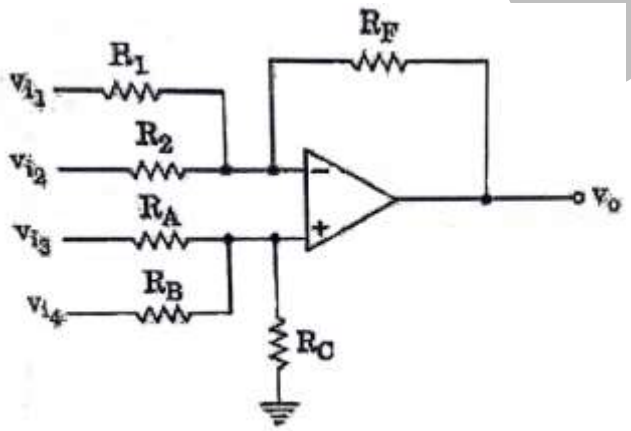


Fig. 8(b)

UPSC – ELECTRICAL Engineering optional – 2019 Questions

1. Find the DC input resistance at the transistor base of the circuit shown in Figure 1(c)**[10M]**

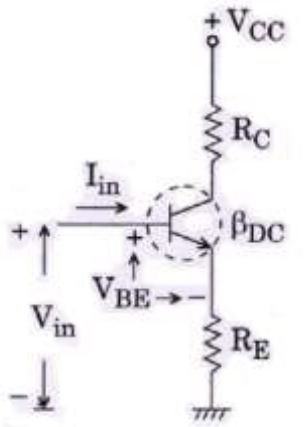


Figure 1

Figure 1(c)

2. Determine the output voltage of the op-amp differentiator circuit shown in Figure 2 for the triangular wave input as shown and draw the output voltage waveform. **[10M]**

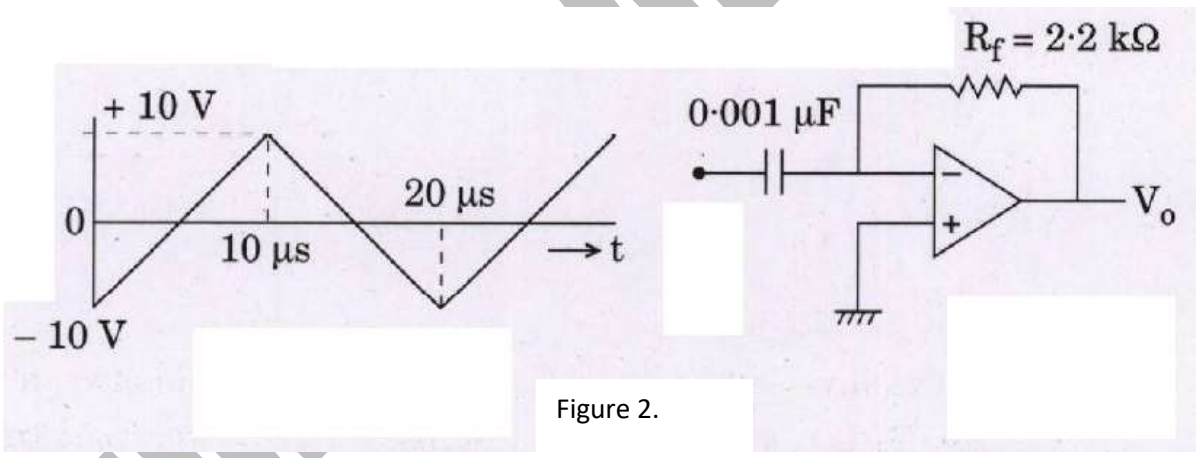


Figure 2.

3. For the circuit shown in Figure 3(c), derive the expression for stability factor S(β).

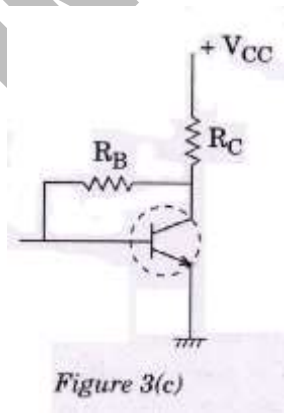


Figure 3(c)

[10M]

4. For the circuit given in Figure 6(d), comment on its operating conditions. **[10M]**

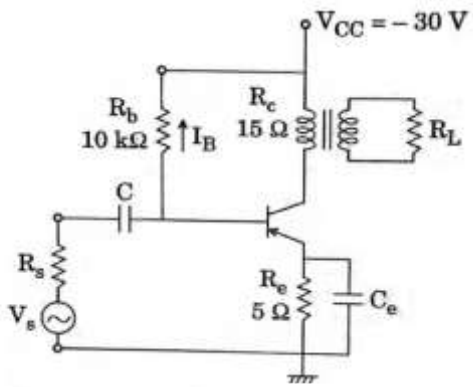


Figure 6(d

For the transistor, $\beta = 100$

$I_{CO} = 1$ mA

(at $V_{CB} = 40$ V)

5. Determine I_D and V_{GS} for the JFET with voltage divider bias as shown in Figure 7(b). The internal parameter values of this JFET are such that $V_D \approx 7V$ **[10M]**

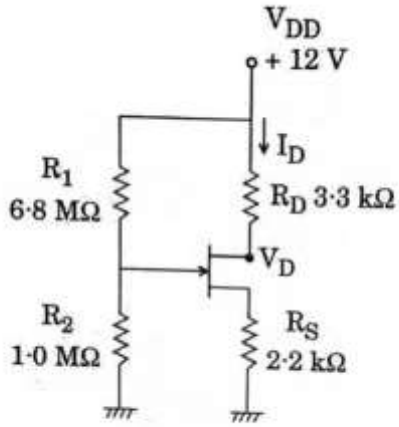


Figure 7(b)

6. A 3-stage amplifier has stages with the following specifications:

Stage	Power Gain	Noise Figure
1	10	2
2	25	4
3	30	5

Calculate the overall power gain and noise figure in dB and the noise temperature. Assume matched conditions. **[10M]**

UPSC – ELECTRICAL Engineering optional – 2020 Questions

1. A Darlington transistor pair circuit is shown in Figure 1 (d) below. Both the transistors have dc current gain β of 30. In the circuit $V_{CC} = +12$ V, $R_E = 1.5\ k\Omega$ **[10M]**

(i) Find the value of R_1 needed to bias the circuit such that $V_{CEQ_2} = 5\ V$ for transistor T_2.

(ii) With the same value of R_1 as obtained above, determine the value of V_{CEQ_1}.

Assume both T_1 and T_2 are Si transistors.

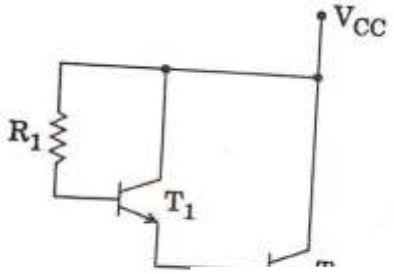


Figure 1

Figure 1(d)

2. Shown below (Figure 3(a)) is a differential amplifier with a three transistor active load. Draw the small signal equivalent circuit of its output stage with active load and calculate its small differential mode voltage gain. Assume the output impedances of the transistors Q_1 to Q_5 to be r_{01} to r_{05} respectively. Assume the base currents to be negligible. **[20M]**

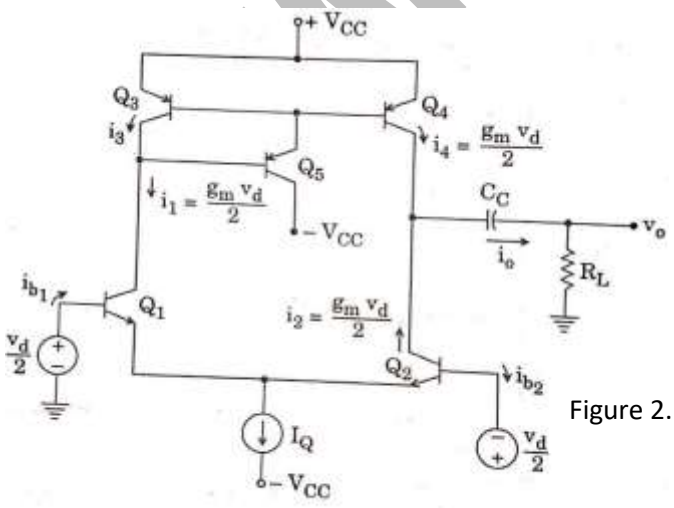


Figure 2.

Figure 3(a)

3. A first order low pass filter circuit is shown in Figure 4 (c) below. It is desired that the dc gain of the filter be 5 and the input impedance is 10 $k\Omega$. The value of the capacitor $C = 100\ nF$. Find the values of R, R_1 and the cut-off frequency f_c of the filter. (Assume ideal OP-AMP) **[10M]**

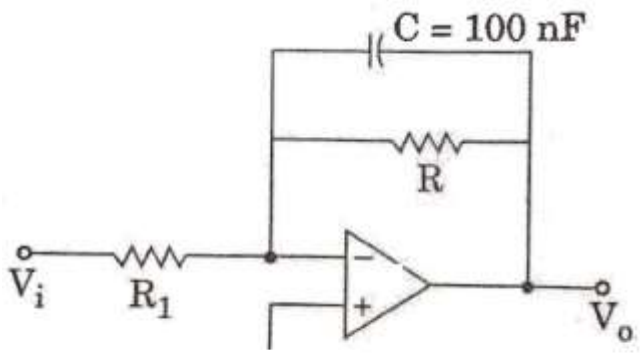


Figure 3.

Figure 4(c)

UPSC – ELECTRICAL Engineering optional – 2021 Questions

1. For the transistor circuit shown in Figure 1(d), determine the value of reverse saturation current, I_S, that would give a collector current of 1 mA, if $\beta = 80, V_A = \infty$ and $V_T = 26\ mV$ at $T = 300\ K$. **[10M]**

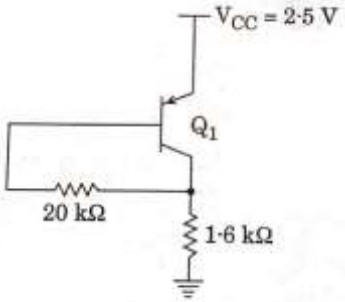


Figure 1(d)

2. Explain what happens when a circuit shown in Figure 3a(i) below is constructed using logarithmic amplifier. **[10M]**

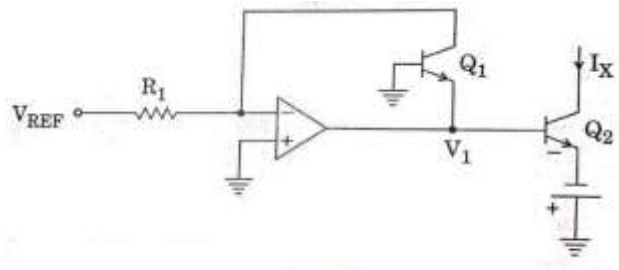


Figure 3(a)(i)

Figure 2.

3. Explain what happens if the topology is modified as shown in Figure 3(a)(ii) below.

[10M]

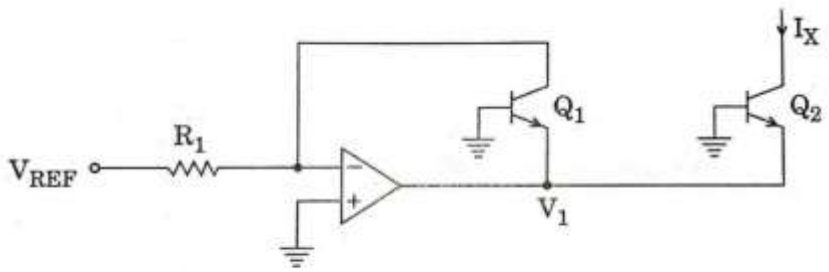


Figure 3(a)(ii)

4. Determine the closed loop gain of the inverting amplifier shown in Figure 4(c) below. Explain the result if $R_1 \to 0$ *or* $R_2 \to 0$. **[10M]**

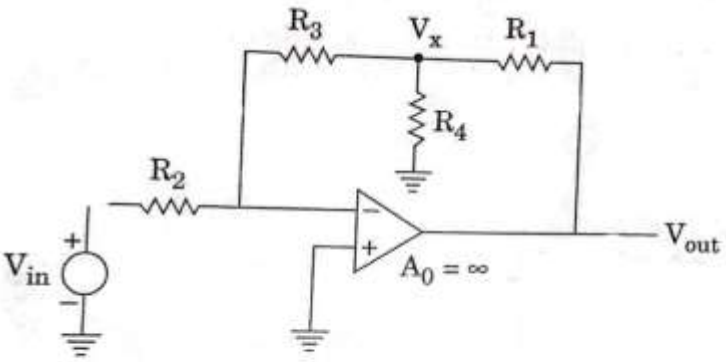


Figure 4(c)